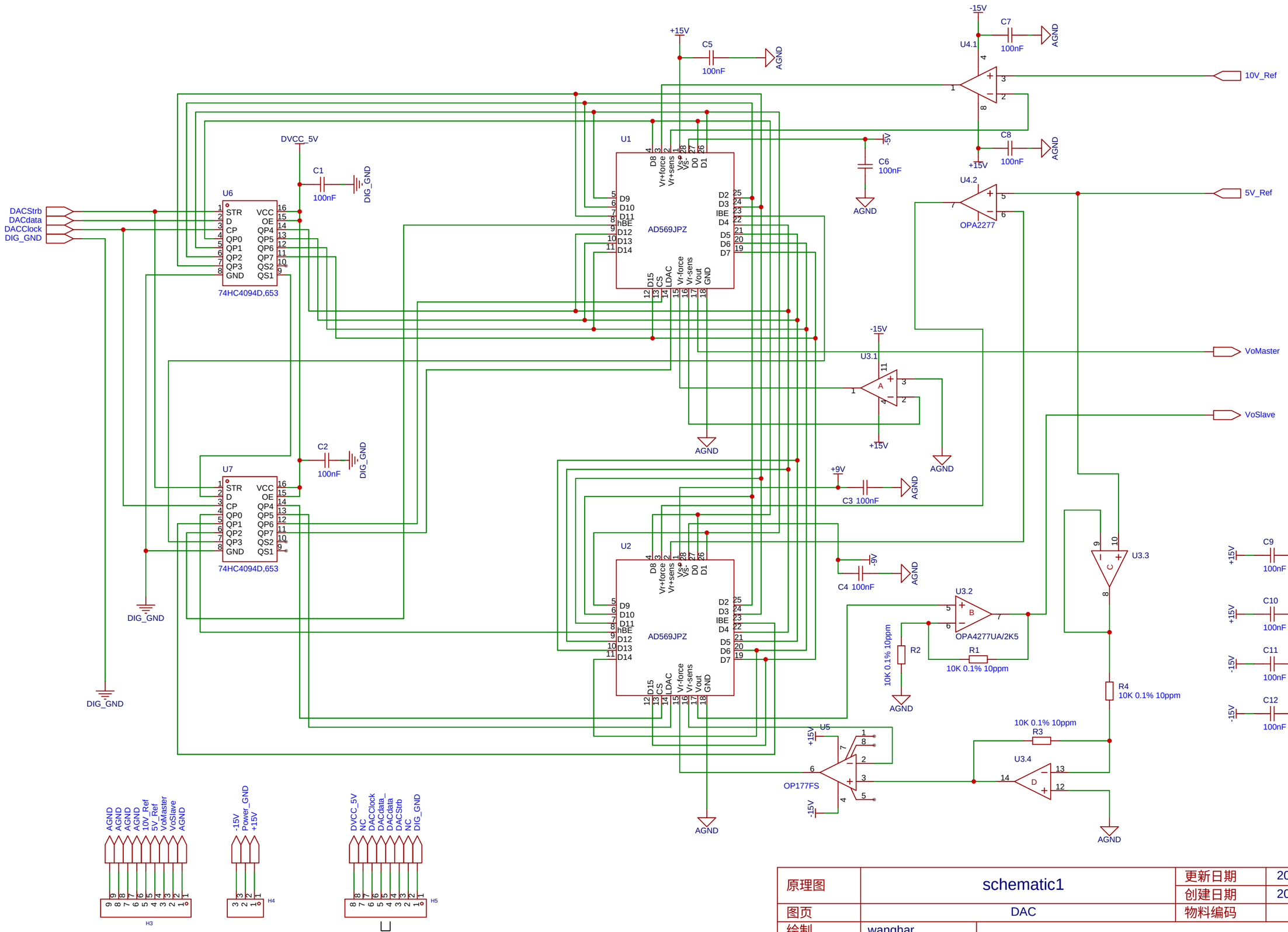


原理图	schematic1	更新日期	2024-04-12
		创建日期	2024-04-12
图页	DAC	物料编码	
绘制	wanghar	Voltgen_V2.1c	
审阅			
		版本	尺寸	页 1 共 5
嘉立创EDA		V1.0	A4	嘉立创EDA

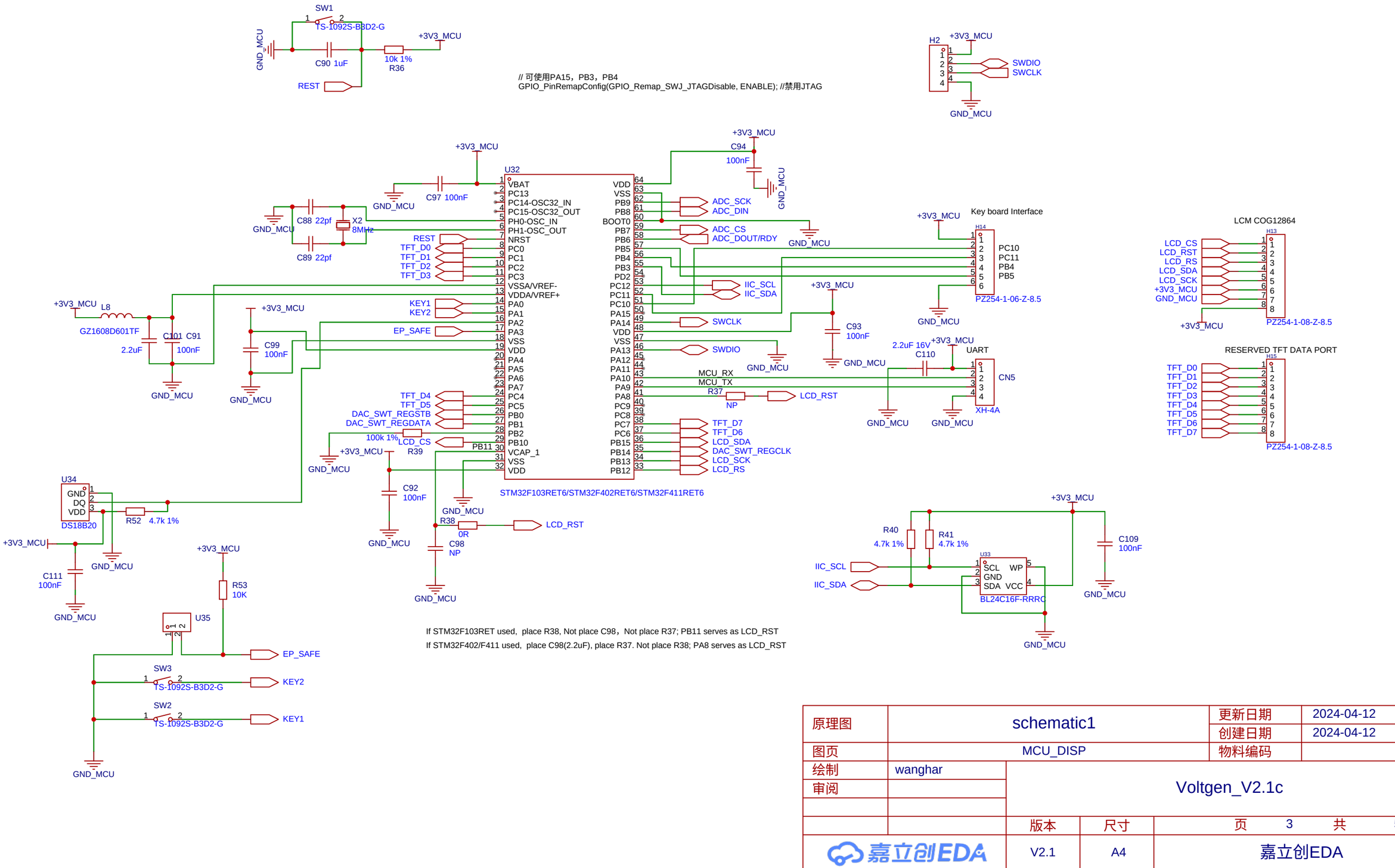
Reserved differential input port: A0A1

IN4(Q0) ->Vout: &b00000001
IN1(Q1) ->StandRef: &b00000010
IN2(Q2) ->Vin_Ext: &b00000100
IN3(Q3) ->AGND: &b00001000

Very critical：C73/C74 capacitance must match X1 very well! (by -2pF)

Shorted @ inner1 layer manually

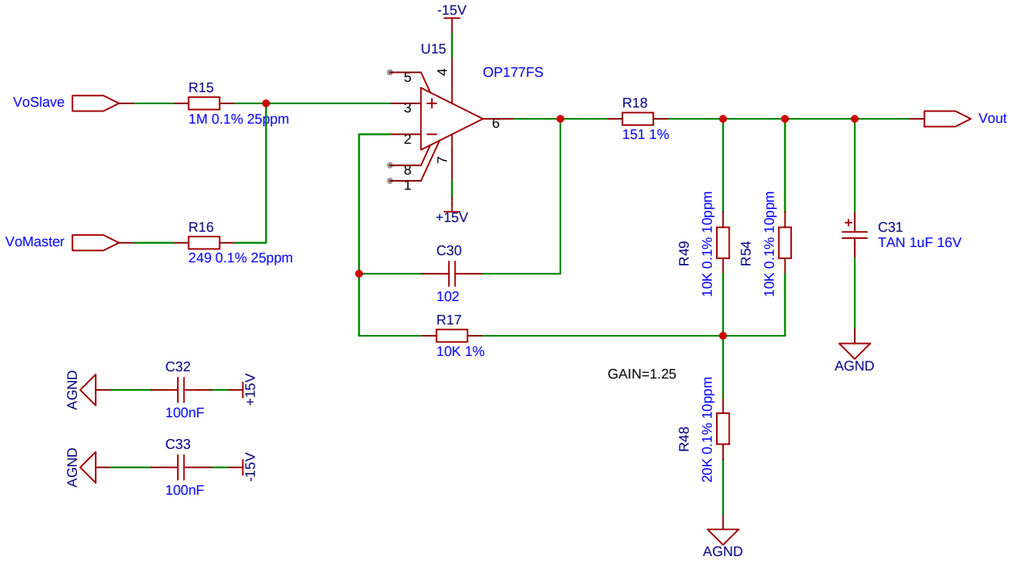
原理图	schematic1	更新日期	2024-04-14
		创建日期	2024-04-12
图页	ADC_SWITCH	物料编码	
绘制	wanghar		
审阅			
		Voltgen_V2.1c	
		版本	尺寸	页 2 共 5
嘉立创EDA		V2.1	A4	嘉立创EDA

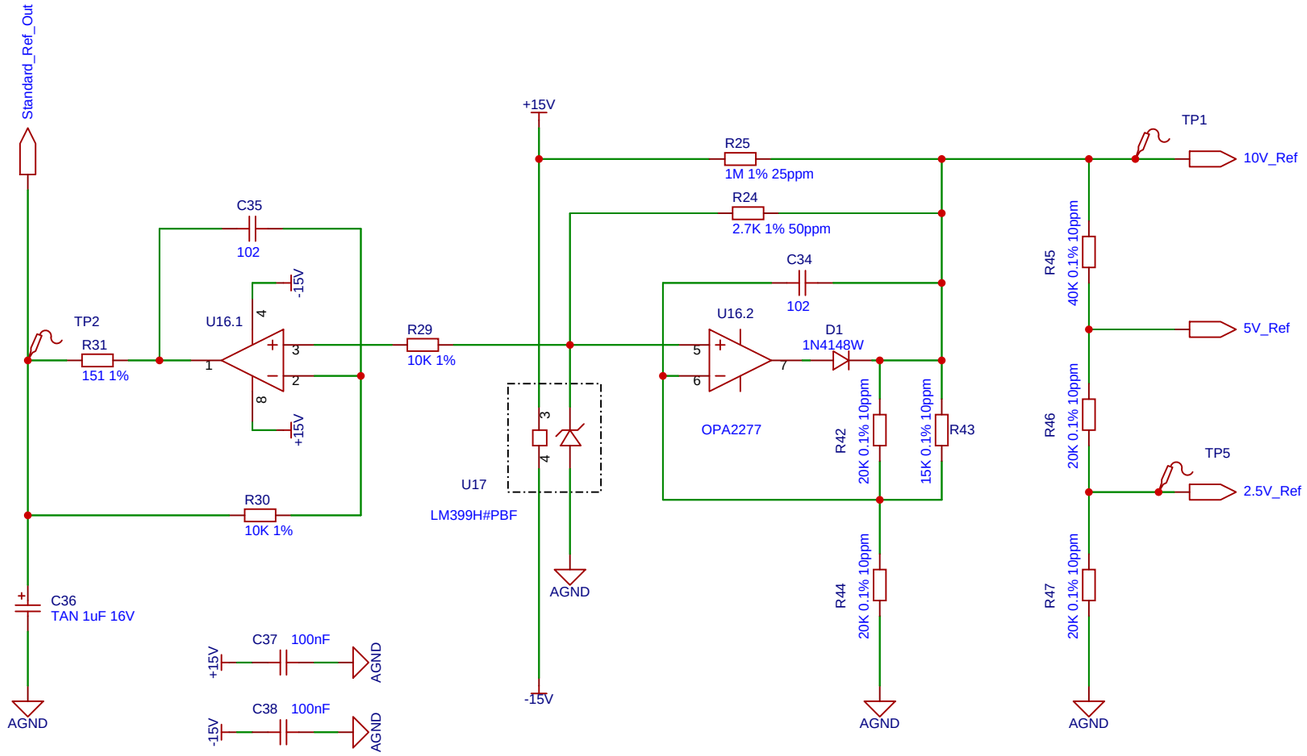


If STM32F103RET used, place R38, Not place C98，Not place R37; PB11 serves as LCD_RST

If STM32F402/F411 used, place C98(2.2uF), place R37. Not place R38; PA8 serves as LCD_RST

原理图	schematic1	更新日期	2024-04-12
		创建日期	2024-04-12
图页	MCU_DISP	物料编码	
绘制	wanghar		
审阅			
		Voltgen_V2.1c	
		版本	尺寸
		V2.1	A4
嘉立创EDA		页 3 共 5	
		嘉立创EDA	





V2.1 Initial release:

-- AD7175-2/AD7177-2 implement

-- MCU selection: 64pin STM32F103RE/STM32F411RE/STM32F402RC

V2.1a correction1: Master AD569,should D8 -> D0, not D8->D1. Done.

V2.1a correction2: AVCC/DVCC/AGND/PGND short caused by copper.Done.

V2.1a correction3: All 0603 footprint is smaller than expectation. No change yet.

V2.1a correction4: Add Key2 @ PA1. Add EPROM_Safe pins @ PA3.

V2.1a correction5: Add 18B20 @ PA2.

V2.1b change AGND/PGND/DGND connection area.

V2.1b add R54,since no easy to get 5K precision res.

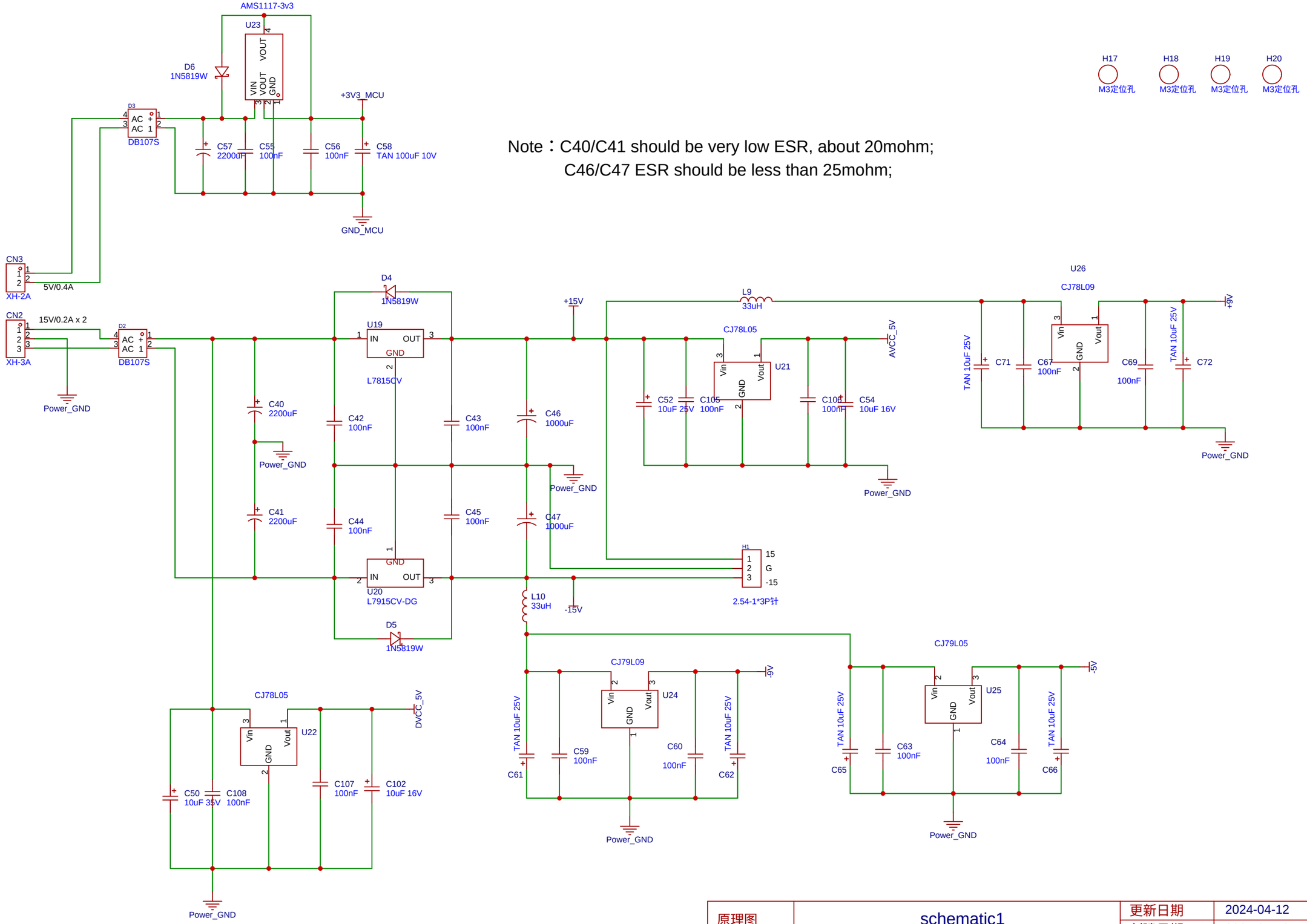
V2.1b add U36, R56/R55, to apply a POSITIVE offset to AGND.

V2.1b add L9/L10.

V2.1c U36/R55/R56 can not resolve the +offset issue; By new added R56/R57 instead.

原理图	schematic1	更新日期	2024-04-12
		创建日期	2024-04-12
图页	Vref_VoltGen	物料编码	
绘制	wanghar	Voltgen_V2.1c	
审阅			
		版本	尺寸
		V1.0	A4

嘉立创EDA



原理图	schematic1	更新日期	2024-04-12
		创建日期	2024-04-12
图页	POWER	物料编码	
绘制	zhengrob	Voltgen_V2.1c	
审阅			
		版本	尺寸
嘉立创EDA		V2.1	A4
		页 5 共 5	
		嘉立创EDA	